IN THE CLAIMS:

1. (Currently amended) A method of swapping out a memory region in a system area network, comprising:

instructing a process to inhibit further operations to the memory region;

determining if a current number of outstanding operations to the memory region is zero; and

swapping out the memory region if the current number of outstanding operations to the memory region is zero, wherein the step of swapping out of the memory region is performed while inhibiting further operations to the memory region.

2. (Currently amended) The method of claim 1, wherein instructing the process to inhibit further operations to the memory region includes setting a ~~quiesce~~ quiescent indicator for the memory region.

3. (Currently amended) The method of claim 2, wherein the ~~quiesce~~ quiescent indicator is located in a fixed memory in association with the memory region.

4. (Currently amended) The method of claim 2, wherein the ~~quiesce~~ quiescent indicator is located in fixed memory in association with a current outstanding operation count for the memory region.

5. (Original) The method of claim 4, wherein determining if a current number of outstanding operations to the memory region is zero includes determining if the current outstanding operation count is zero.

6. (Original) The method of claim 1, wherein swapping out the memory region includes setting a valid bit in a protection table entry associated with the memory region to indicate the memory region is invalid.

7. (Original) The method of claim 1, wherein swapping out the memory region includes deregistering the memory region.

8. (Original) The method of claim 1, further comprising:

swapping in the memory region;

updating an address translation table based on the swapping in of the memory region.

9. (Currently amended) The method of claim 2, further comprising:

swapping in the memory region; and

resetting the ~~quiesce~~ quiescent indicator to allow further operations to the memory region.

10. (Original) The method of claim 6, further comprising:

swapping in the memory region; and

resetting the valid bit to indicate the memory region is valid.

11. (Currently amended) A computer program product in a computer readable medium for swapping out a memory region in a system area network, comprising:

first instructions for instructing a process to inhibit further operations to the memory region;

second instructions for determining if a current number of outstanding operations to the memory region is zero; and

third instructions for swapping out the memory region if the current number of outstanding operations to the memory region is zero, wherein the step of swapping out of the memory region is performed while inhibiting further operations to the memory region.

12. (Currently amended) The computer program product of claim 11, wherein the first instructions for instructing the process to inhibit further operations to the memory

region include instructions for setting a ~~quiesce~~ quiescent indicator for the memory region.

13. (Currently amended) The computer program product of claim 12, wherein the ~~quiesce~~ quiescent indicator is located in a fixed memory in association with the memory region.

14. (Currently amended) The computer program product of claim 12, wherein the ~~quiesce~~ quiescent indicator is located in fixed memory in association with a current outstanding operation count for the memory region.

15. (Original) The computer program product of claim 14, wherein the second instructions for determining if a current number of outstanding operations to the memory region is zero include instructions for determining if the current outstanding operation count is zero.

16. (Original) The computer program product of claim 11, wherein the third instructions for swapping out the memory region include instructions for setting a valid bit in a protection table entry associated with the memory region to indicate the memory region is invalid.

17. (Original) The computer program product of claim 11, wherein the third instructions for swapping out the memory region include instructions for deregistering the memory region.

18. (Original) The computer program product of claim 11, further comprising:

fourth instructions for swapping in the memory region;

fifth instructions for updating an address translation table based on the swapping in of the memory region.

19. (Currently amended) The computer program product of claim 12, further comprising:

fourth instructions for swapping in the memory region; and

fifth instructions for resetting the ~~quiesce~~ quiescent indicator to allow further operations to the memory region.

20. (Currently amended) The computer program product of claim 16, further comprising:

fourth ~~instracions~~ instructions for swapping in the memory region; and

fifth instructions for resetting the valid bit to indicate the memory region is valid.

21. (Currently amended) An apparatus for swapping out a memory region in a system area network, comprising:

means for instructing a process to inhibit further operations to the memory region;

means for determining if a current number of outstanding operations to the memory region is zero; and

means for swapping out the memory region if the current number of outstanding operations to the memory region is zero, wherein the step of swapping out of the memory region is performed while inhibiting further operations to the memory region.

22. (Currently amended) The apparatus of claim 21, wherein the means for instructing the process to inhibit further operations to the memory region includes means for setting a ~~quiesce~~ quiescent indicator for the memory region.

23. (Currently amended) The apparatus of claim 22, wherein the ~~quiesce~~ quiescent indicator is located in a fixed memory in association with the memory region.

24. (Currently amended) The apparatus of claim 22, wherein the ~~quiesce~~ quiescent indicator is located in fixed memory in association with a current outstanding operation count for the memory region.

25. (Original) The apparatus of claim 24, wherein the means for determining if a current number of outstanding operations to the memory region is zero includes means for determining if the current outstanding operation count is zero.

26. (Original) The apparatus of claim 21, wherein the means for swapping out the memory region includes means for setting a valid bit in a protection table entry associated with the memory region to indicate the memory region is invalid.

27. (Original) The apparatus of claim 21, wherein the means for swapping out the memory region includes means for deregistering the memory region.

28. (Original) The apparatus of claim 21, further comprising:
means for swapping in the memory region;
means for updating an address translation table based on the swapping in of the memory region.

29. (Currently amended) The apparatus of claim 22, further comprising:
means for swapping in the memory region; and
means for resetting the ~~quiesce~~ quiescent indicator to allow further operations to the memory region.

30. (Original) The apparatus of claim 26, further comprising:
means for swapping in the memory region; and
means for resetting the valid bit to indicate the memory region is valid.